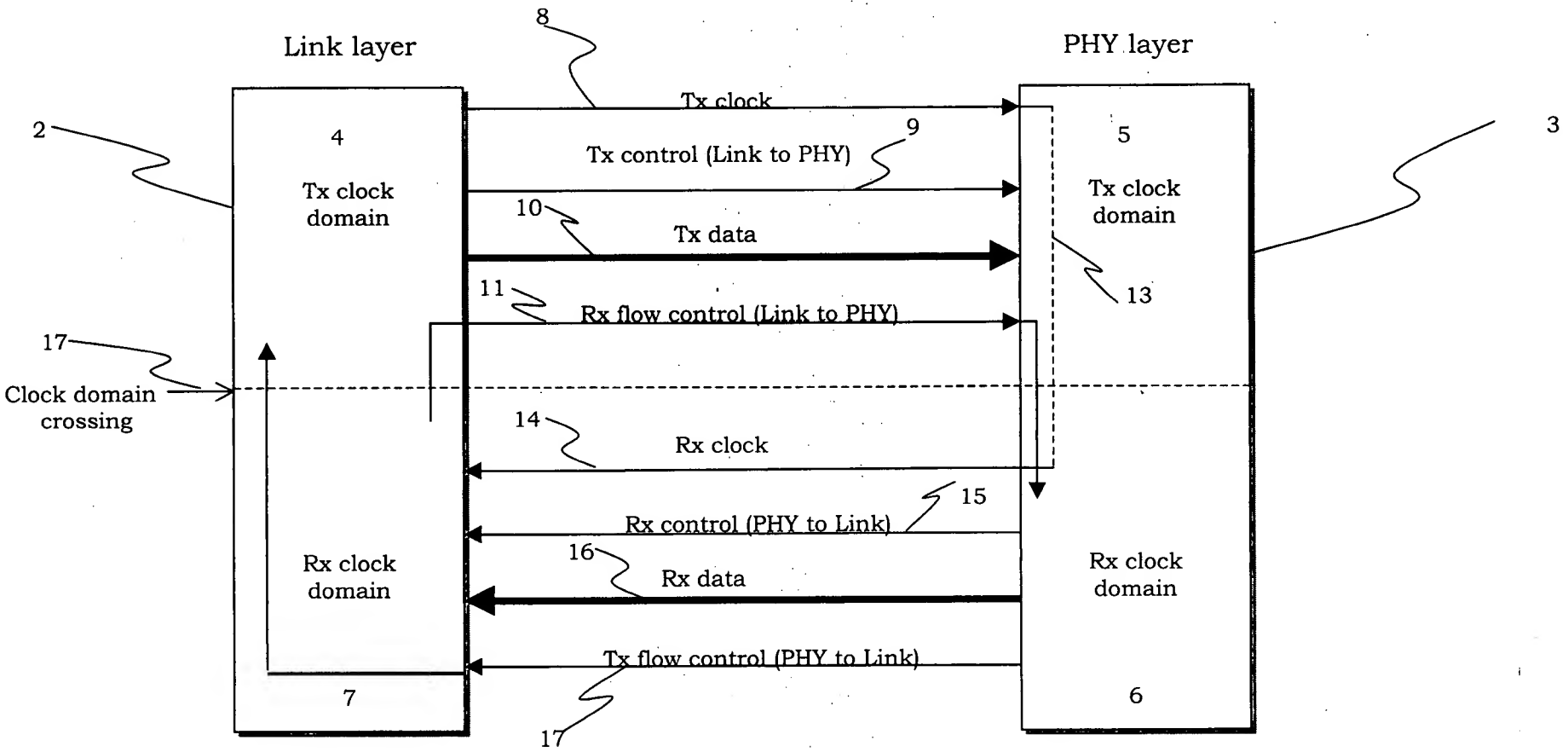

Link layer
PHY layer
8
Tx clock
2
4
Tx clock domain
9
Tx control (Link to PHY)
5
Tx clock domain
3
10
Tx data
13
11
Rx flow control (Link to PHY)
17
Clock domain crossing
14
Rx clock
15
Rx control (PHY to Link)
16
Rx data
Rx clock domain
Rx clock domain
Tx flow control (PHY to Link)
7
6
17
1

FIGURE 1

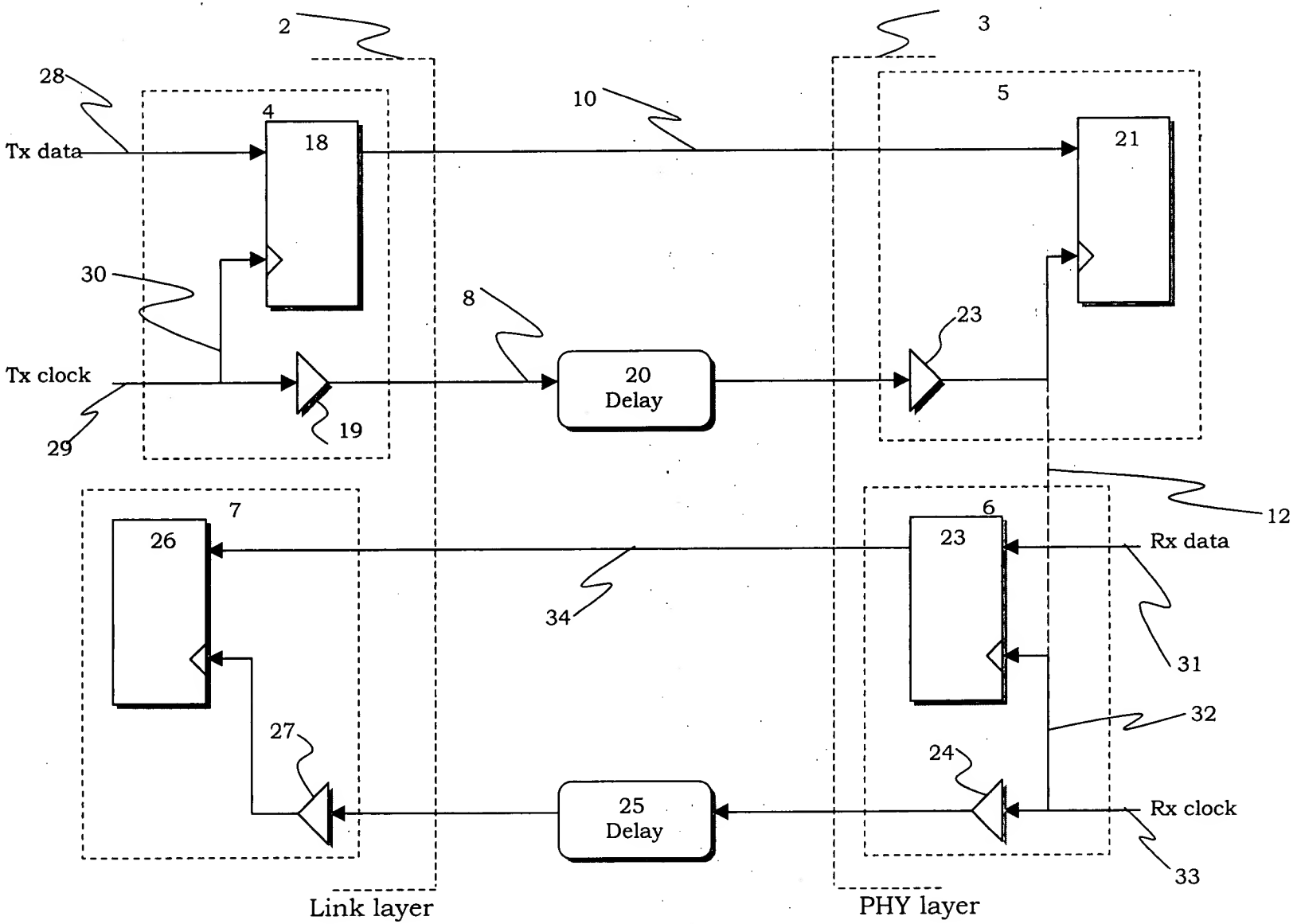


FIGURE 2

09450802 .112999

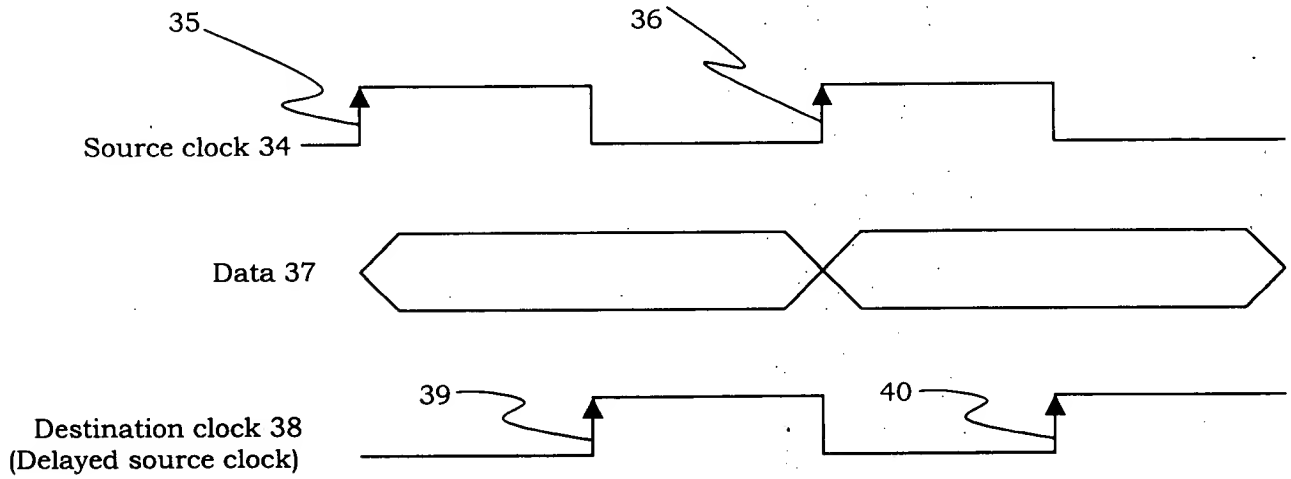
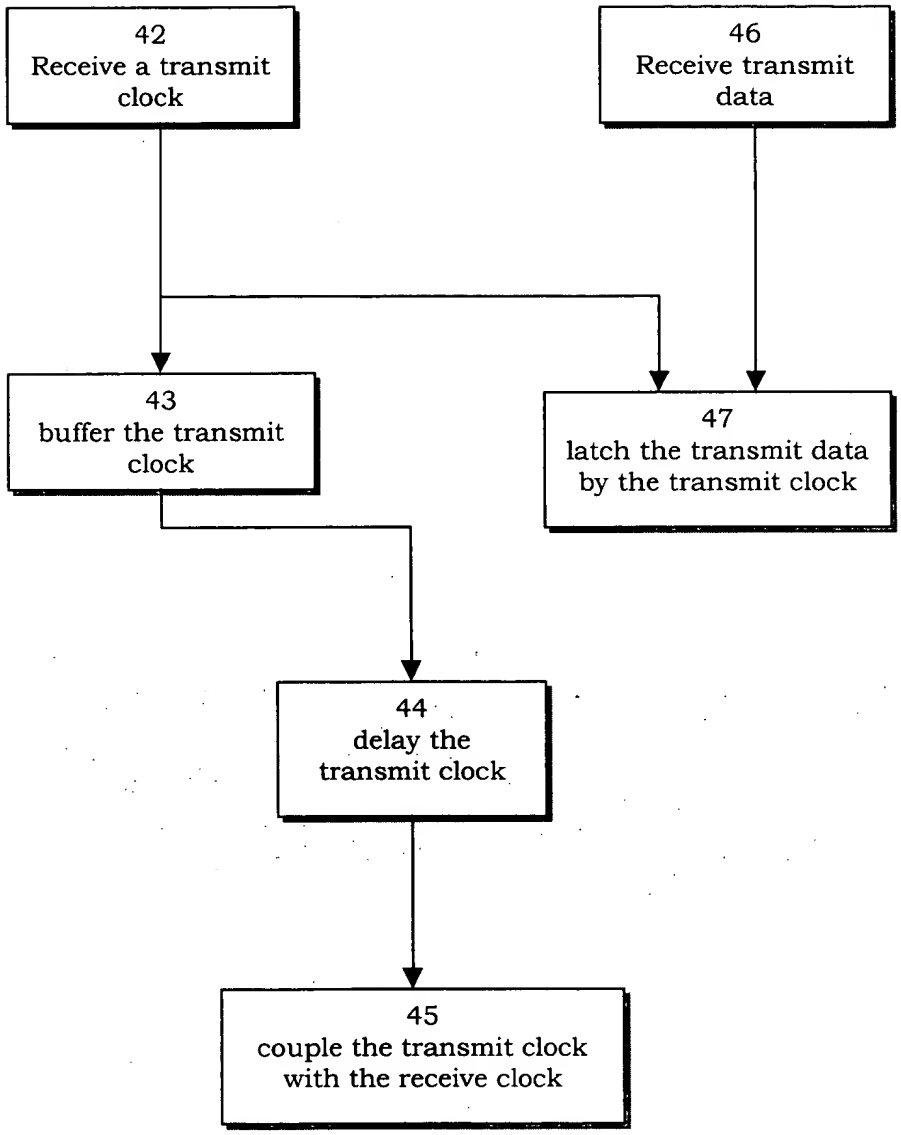
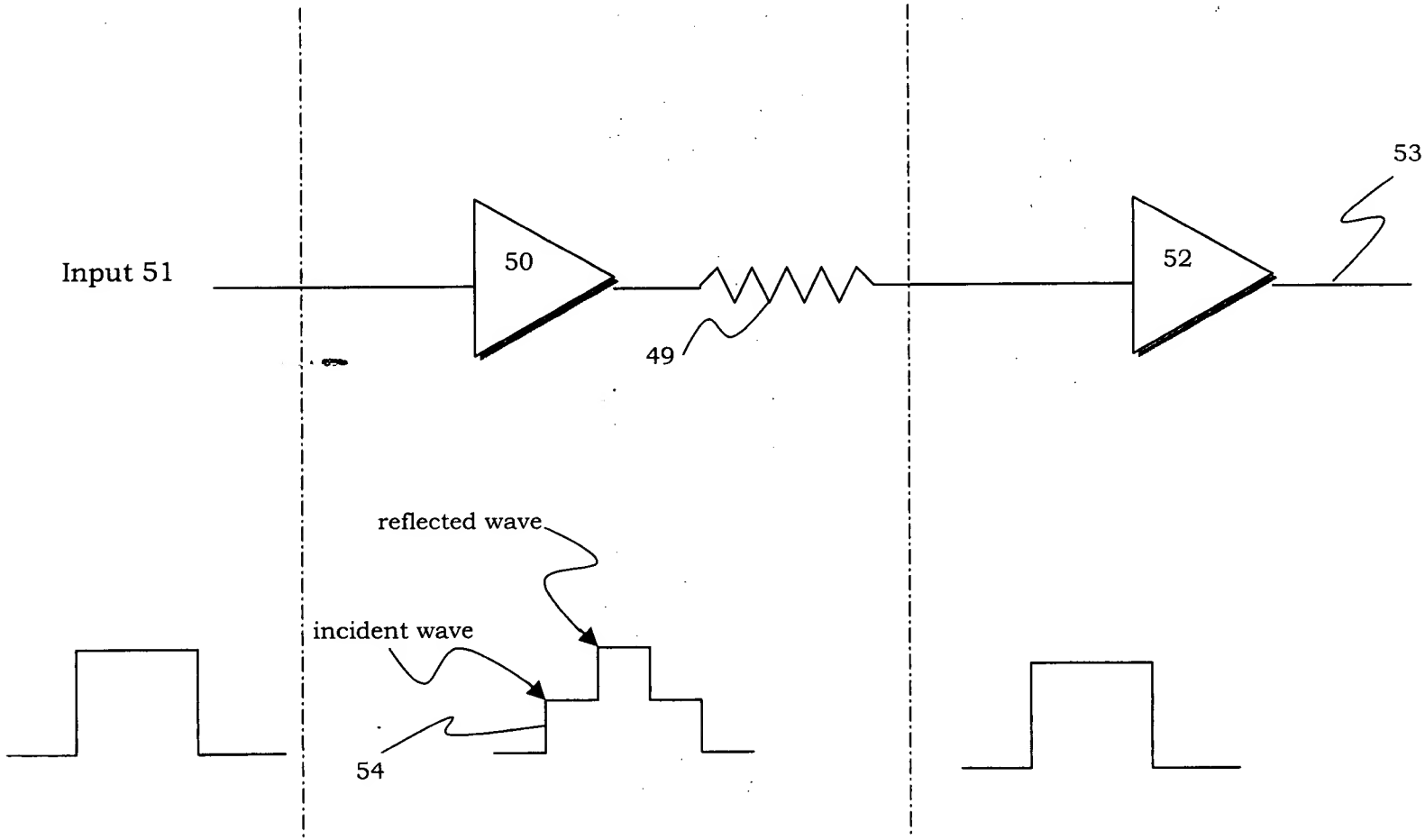

35
36
Source clock 34
Data 37
39
40
Destination clock 38
(Delayed source clock)

FIGURE 3


42
Receive a transmit clock
46
Receive transmit data
43
buffer the transmit clock
47
latch the transmit data by the transmit clock
44
delay the transmit clock
45
couple the transmit clock with the receive clock

41

FIGURE 4



48

FIGURE 5